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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/930,847	08/14/2001	Po-Sheng Shih	JCLA6974	2113

7590 03/06/2003

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EXAMINER	
LEWIS, MONICA	
ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 03/06/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/930,847	SHIH, PO-SHENG	
	Examiner	Art Unit	
	Monica Lewis	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence addr ss --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 January 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *15-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This action is in response to the amendment filed January 2, 2003.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as obvious over Applicant's Prior Art Drawings in view of Wu (U.S. Patent No. 5,977,561) and Cho et al. (U.S. Patent No. 5,578,838).

In regards to claim 15, Applicant's Prior Art Drawings disclose the following:

a) an insulating substrate (100) (See Figure 1b);

b) a polysilicon layer over the substrate (104) (See Figure 1b); and

c) a gate structure over the polysilicon layer, wherein the gate structure includes a gate layer (108), a gate dielectric layer (106) between the gate layer and the polysilicon layer (See Figure 1b).

In regards to claim 15, Applicant's Prior Art Drawings fails to disclose the following:

a) a spacer on each side of the gate layer, wherein the spacer with respect to a surface of the gate dielectric layer and a surface of the polysilicon layer forms a contrast surface.

However, Wu discloses a semiconductor device that has a spacer (24) on each side (See Figure 7). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Applicant's Prior Art Drawings to

include a spacer as disclosed in Wu because it aids in isolating the gate, source and drain regions (See Figure 7).

Additionally, since Applicant's Prior Art Drawings and Wu are both from the same field of endeavor, the purpose disclosed by Wu would have been recognized in the pertinent art of Applicant's Prior Art Drawings.

b) a selective conductive layer serves as a source/drain region without additionally implanting process on the source/drain region.

However, Cho et al. ("Cho") discloses a semiconductor device that has a conductive layer (14) that functions as a source/drain region (See Figure 4 and Column 4 Lines 53-55). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Applicant's Prior Art Drawings to include a conductive layer as disclosed in Cho because it aids in providing a connection among the layers (See Figure 4, Column 3 Lines 3-15 and Column 4 Lines 53-55).

Additionally, the limitation of "a source/drain region without additionally implanting process on the source/drain region" makes it a product by process claim. The MPEP § 2113, states, "Even though product -by[-] process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process." *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985)(citations omitted).

A *"product by process"* claim is directed to the product per se, no matter how actually made, *In re Hirao and Sato et al.*, 190 USPQ 15 at 17 (CCPA 1976) (footnote 3). See also *In re Brown and Saffer*, 173 USPQ 685 (CCPA 1972): *In re Luck and Gainer*, 177 USPQ 523 (CCPA 1973); In re Fessmann, 180 USPQ 324 (CCPA 1974); and *In re Marosi et al.*, 218 USPQ 289 (CAFC 1983) final product per se which must be determined in a *"product by, all of"* claim, and not the patentability of the process, and that an old or obvious product, whether claimed in *"product by process"* claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

Finally, since Applicant's Prior Art Drawings and Cho are both from the same field of endeavor, the purpose disclosed by Cho would have been recognized in the pertinent art of Applicant's Prior Art Drawings.

In regards to claim 16, Applicant's Prior Art Drawings disclose the following:

a) the polysilicon layer has a thickness between about 250A to 350A (See Page 2 Lines 11-12).

Additionally, the applicant has not established the critical nature of "the polysilicon layer has a thickness between about 250A to 350A." "The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims. . . . In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range." *In re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir.1990).

4. Claim 17 is rejected under 35 U.S.C. 103(a) as obvious over Applicant's Prior Art Drawings in view of Wu (U.S. Patent No. 5,977,561), Cho et al. (U.S. Patent No. 5,578,838) and Kawachi et al. (U.S. Patent No. 6,104,040).

In regards to claim 17, Applicant's Prior Art Drawings fails to disclose the following:

a) the conductive layer includes an in-situ doped silicon-germanium (SiGe) layer.

However, Kawachi et al. ("Kawachi") discloses a semiconductor device that has a thin film transistor with a SiGe conductive layer (See Column 2 Lines 51-55 and Column 7 Lines 22-28). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Applicant's Prior Art Drawings to include a SiGe layer as disclosed in Kawachi because it aids in lowering the threshold voltage (See Column 7 Lines 22-28).

Additionally, since Applicant's Prior Art Drawings and Kawachi are both from the same field of endeavor, the purpose disclosed by Kawachi would have been recognized in the pertinent art of Applicant's Prior Art Drawings.

5. Claims 18 and 19 are rejected under 35 U.S.C. 103(a) as obvious over Applicant's Prior Art Drawings in view of Wu (U.S. Patent No. 5,977,561), Cho et al. (U.S. Patent No. 5,578,838) and Nakajima et al. (U.S. Patent No. 6,118,140).

In regards to claim 18, Applicant's Prior Art Drawings fails to disclose the following:

a) the conductive layer is tungsten.

However, Nakajima et al. ("Nakajima") discloses a semiconductor device that has conductive layer of tungsten (See Column 19 Lines 4-10). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor

device of Applicant's Prior Art Drawings to include a tungsten layer as disclosed in Nakajima because it aids in providing a connection among the layers (See Figure 29).

Additionally, since Applicant's Prior Art Drawings and Nakajima are both from the same field of endeavor, the purpose disclosed by Nakajima would have been recognized in the pertinent art of Applicant's Prior Art Drawings.

In regards to claim 19, Applicant's Prior Art Drawings fails to disclose the following:

a) the conductive layer is metal silicide.

However, Nakajima discloses a semiconductor device that has conductive layer of metal silicide (See Column 19 Lines 4-10). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Applicant's Prior Art Drawings to include a metal silicide layer as disclosed in Nakajima because it aids in providing a connection among the layers (See Figure 29).

Additionally, since Applicant's Prior Art Drawings and Nakajima are both from the same field of endeavor, the purpose disclosed by Nakajima would have been recognized in the pertinent art of Applicant's Prior Art Drawings.

6. Claim 20 is rejected under 35 U.S.C. 103(a) as obvious over Applicant's Prior Art Drawings in view of Wu (U.S. Patent No. 5,977,561), Cho et al. (U.S. Patent No. 5,578,838) and Gardner et al. (U.S. Patent No. 5,872,376).

In regards to claim 20, Applicant's Prior Art Drawings fails to disclose the following:

a) the spacer is a tetra-ethyl-ortho-silicate (TEOS) layer.

However, Gardner et al. ("Gardner") discloses a semiconductor device that has spacer comprised of TEOS (See Column 6 Lines 54-67 and Column 7 Lines 1-3). It would have been

obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Applicant's Prior Art Drawings to include a spacer layer as disclosed in Gardener because it aids in isolating the gate, source and drain regions (See Column 6 Lines 54-67 and Column 7 Lines 1-3).

Response to Arguments

7. Applicant's arguments filed January 2, 2003 have been fully considered but they are not persuasive. First, Applicant argues that "the spacer 208 of the present invention has different function from the spacer 24 disclosed by Wu. The two spacers with respect to the present invention and Wu are not equivalent." However, there are no limitations in the claims that would indicate that the spacers are not the same.

Second, Applicant argues that "the semiconductor layer 14 is also not equivalent to the conductive layer 210 of the present invention. It should be noted that the conductive layer 210 of the present invention is selectively form on the polysilicon layer 202 (but not the insulation layer 13 for Cho et al.). Also and, the present invention needs no additional implanting process." However, there are no limitations in the claims that would indicate that the conductive layers are not the same. Additionally, Cho as stated above discloses a conductive layer (14) that serves as a source/drain region (See Figure 4 and Column 4 Lines 53-55). Finally, as stated above the limitation of "a source/drain region without additionally implanting process on the source/drain region" makes it a product by process claim. Therefore, Applicant's arguments are not persuasive.

Conclusion

8. The following prior art made of record and not relied upon is considered pertinent to applicant's disclosure: a) Hsu et al. (U.S. Patent No. 5,663,578) discloses a thin film transistor.

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica Lewis whose telephone number is 703-305-3743. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 703-308-4905. The fax phone number for the organization where this application or proceeding is assigned is 703-308-7722 for regular and after final

communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

ML

February 28, 2003

AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800